LEVEL II

Final Technical Report

September 30,1977 through September 29,1979

SINGLE CHIP LENSES FOR ULTRASONIC IMAGING

Amended

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Sponsored by

Advanced Research Projects Agency (DOD)
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During this program, the theoretical understanding of Cascade Charge Coupled Device (C3D) electronic lenses have been greatly extended. Specifically, the attenuation effects of transfer efficiency were found to be deterministic and insignificant, lateral resolution and sidelobe response were found not to be serious limitations, while for moderate values of charge-transfer inefficiency, spatial shifting of beamsteering angle was found to be minor. In addition, a novel analysis of the device performance substantiated that aberations resulting from the intermodulation process would, in most practical cases, not limit

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system performance. Also during this program, the fabrication process for the device was optimized. This includes optimizing of the polysilicon electrode conduction and the channel length. An advanced lens incorporating the cumulative design rules resulting from this program has been fabricated. This device, a 32 channel, 10,000 charge-coupled element lens, will be used in 4.5 MHz imaging system to be developed under another program.

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REPORT SUMMARY

During the two years of sponsorship the theoretical understanding of Cascade Charge Coupled Device (C3D) electronic lenses have been greatly extended. Specifically the effects of the intermodulation products, sidelobe resoluion limitations, transfer inefficiencies are now better understood as a result of this program. Additionally a second generation device that has both beam steer and focus sections has been fabricated and used to test the validity of the performance models that have been derived. A third generation device has been recently fabricated that includes three beam steer section pairs and one focus section. This advanced lens incorporates the cumulative design rules resulting from this research program. It is anticipated that this 32 channel, 10,000 charge-coupled element lens, will be used in a 4.5 MHz imaging system to be developed under other funding.

I. SUMMARY OF RESULTS

This report covers the work performed during a two year period of sponsorship. The research performed involved the modelling and fabrication of an novel integrated circuit time delay and signal summing element called a Cascade Charge Coupled Device (C3D). Although the device had been invented under previous sponsorship of another agency not enough research had been performed in order to predict the performance of a given lens design. These two years of modelling and fabrication sponsorhip have enabled a much greater understanding of the capability of the C3D lens and how it is to be optimized for a specific application. Although the use of multi-channel delay-add is generic to a wide class of electronic signal processing applications, the specific application of interest to the authors is the use of the device for beamsteering and focussing of signals for acoustic transducer arrays.

Specifically during the first year the emphasis was on modelling and fabrication process development for the third generation lens. The second generation lens that was anticipated to be fabricated in this first year was actually fabricated prior to the beginning of this program due to delays in the start of sponsorship. Extensive modelling work on transfer efficiency was performed and reported in the previous semi annual reports of the first year. In summary it was found: (1) the attenuation effects of transfer efficiency are deterministic and insignificant, (2) the

lateral resolution and sidelobe response are to first order not modified, and (3) for moderate values of charge-transfer inefficiency the spatial shifting of the beamsteering angle is minor. Thus the C3D is largely insensitive to the major limitation commonly encounterd (transfer inefficiency) in charge coupled device applications today. A comprehensive coverage of this analysis is presented in the Stanford University doctoral thesis of John Shott. A complete reprint of this dissertation is publicly available through the University of Michigan Archives for a nominal reproduction charge. Appendix A of this report contains the analysis of the fundamentals of C3D performance found in Chapter 5 of John Shott's dissertation.

The fabrication process development of the first year concentrated on polysilicon electrode and insulating silicon oxide formation. Test fabrication runs were made to optimize further the design parameters of channel length and polysilicon electrode conductance. The channnel length studies concerned experiments in electrode etching technolgies. The previously used etchants were originally developed for optical sensors with no significant constraints on etching small geometries. The difficulties experienced with small geometry electrode (5 micron lines) etching were associated with bubbles that formed on the surface being etched. These bubbles radically enhanced the etch rate in their vicinity by over an order of magnitude. The etching process developed by Ernie Wood circumvented this problem by

scrubbing the surface of the wafers during etching with a high flow rate of nitrogen gas bubbles. The action of the bubbles on the surface increased the uniformity of the etch by preventing bubbles formed during the etching process from modifying one region etch rate while regions without bubbles etched at a different rate. The etching process provided reproducible five micron line and space etching. The parameters of the etching process were empirically derived using a qualitative success criteria. This fabrication research was not performed under ARPA sponsorship. Alternative sponsorhip was necessary as a result of the greatly reduced budget for the second year of work from that which had been originally planned. Fabrication research was supported by other sources to make funds available to purchase the spectrum analyser required for the second years work. The details of these etching technologies will be made available in the open literature in the dissertation of Mr. Wood.

During the second year of funding additional modelling of the inter-modulation products was performed, the third generation C3D lens design was completed and fabrication runs were performed on a device test chip. A spectrum analyser was purchased to perform critical measurements in the the verification of the intermodulation product model. This instrument has proven invaluable in making spectral measurements.

The intermodulation product modelling was concerned with

the effects on performance resulting from the direct connection of two charge coupled device section operating at different frequencies without the conventional lowpass antialiasing filters commonly used in sampled data systems. Michael Eaton developed a simple analysis technique using orthogonal deconvolution of the problem into two parts. This novel analysis method was described in the third semiannual report and in much more detail in his Stanford University doctoral dissertation. This analysis from Chapter IV of Dr. Eaton's dissertation is repeated in in Appendix B of this report. The results of this analysis substantiate that the abberations resulting from the intermodulation process will in most practical cases not limit system performance.

The fabrication work, though extensive, is not as easily summarized by few words. Perhaps the most impressive summary that made is obtained by studying the third generation C3D design layout shown in Fig. 1 and the photomicrograph of the 10,000 element, 32 channel device shown in Fig. 2. This C3D represents the most complex integrated circuit device ever fabricated in the Stanford University Integrated Circuits Laboratory, a laboratory well known throughout the world as the recipient of more outstanding paper awards at the International Solid State Circuits Conference than other university laboratory. This complex C3D is more than a test structure to verify intermodulation research models developed under the sponsorship of this grant. It is a complete third generation lens capable of imaging using 4.5

MHz ultrasound. While this grant concerned the modeling of intermodulation distortion and other performance limits of C3D lenses, the fabrication techniques, the C3D design techniques, and the application tradeoff analysis were developed under parallel funding. The results of this research will be made available to other researchers in the forthcoming doctoral dissertation of Ernie Wood.

While funding of this work has been carried out under the sponsorship of the Advanced Projects Research Agency, the majority of sponsorship of the doctoral programs of Shott, Eaton, and Wood were derived from other sponsor interested in the application of the C3D lens to a specific application.

II. List of Relevant Dissertations

A. John Shott, "Charge-Coupled Devices for Use in Electronically Focused Ultrasonic Imaging Systems", May 1978, Stanford University.

B. Michael Eaton, "High Performance Preprocessor Electronics for Ultrasonic Imaging", May 1979, Stanford Unversity.

C. Ernie Wood, in preparation anticipated June, 1981

III. Personnel Involved in the Research

A. James D. Meindl, Principal Investigator

B. Roger D. Melen, Program Manager

C. John D. Shott, Research Assistant

D. Michael Eaton, Research Assistant

E. Ernie Wood, Research Assistant

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IV. COUPLING ACTIVITIES WITH OTHER RELATED RESEARCH

The most significant coupling with other ARPA research in related activies concerns our extensive interrelationship with the research activies of Professor Gordon Kino of the Stanford University Ginston Laboratory. Professor Kino has long-term interest in the technologies used in the nondestructive inspection of materials (NDI). This research effort and those of Professor Kino have benefitted through both formal research meetings and informal discussions between students and researchers.

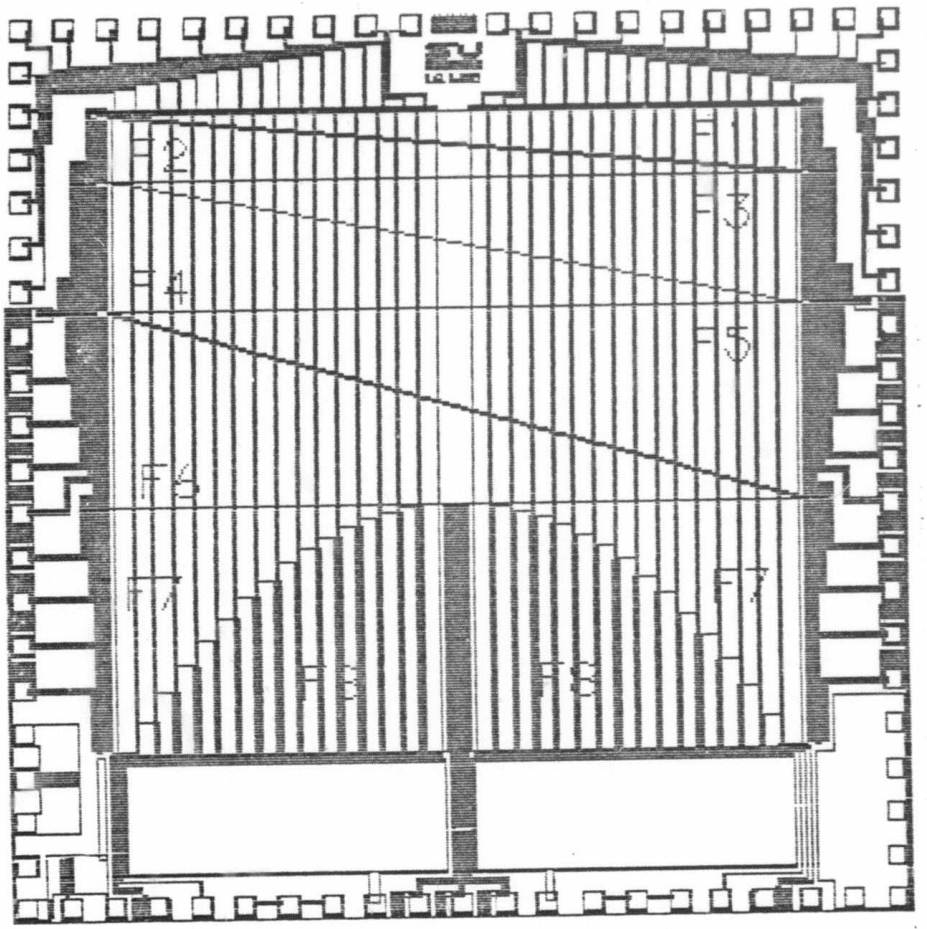

Fig. 1 Computer-assisted layout of 32 channel C3D lens

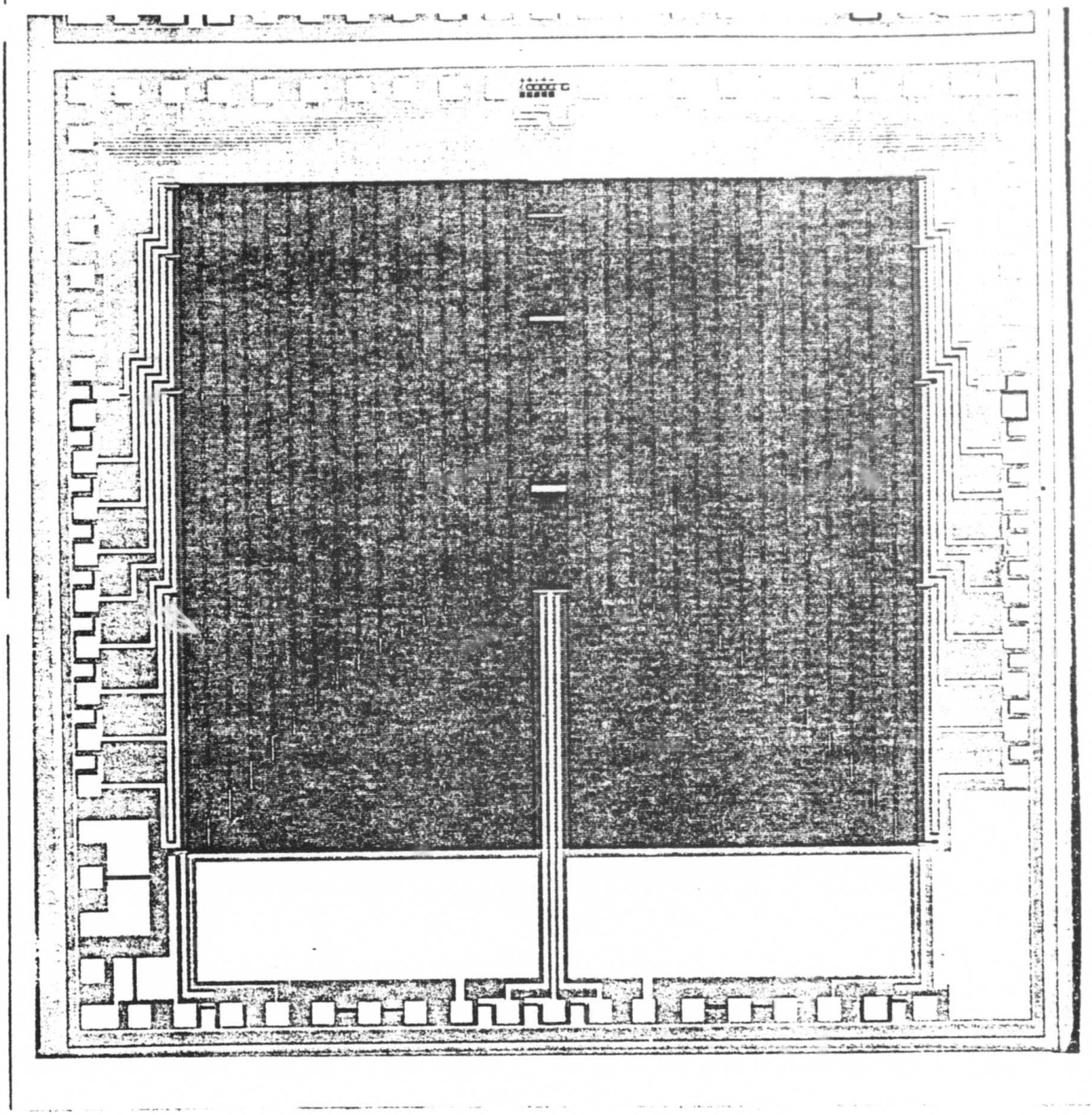

Fig. 2 Photomicrograph of 32 channel, 10,000 element C3D lens

APPENDIX A: Chapter 5 of John Shott's Ph.D. Dissertation

FUNDAMENTAL LIMITS OF C3D PERFORMANCE

The time-delay accuracy of the cascade charge-coupled device will largely determine its ultimate utility as an electronic lens for an ultrasonic imaging system. Time-delay and amplitude errors can reduce overall image quality by creating uncertainty as to the position of the focal point of the lens or by degrading the sidelobe level of the image. As a result, this chapter examines the aspects of the C3D electronic lens that will inherently limit the time-delay and amplitude accuracy generated by this approach.

The effects of incomplete charge transfer on the imaging system are considered in Section A. The remainder of this chapter discusses the limitations imposed by including a number of independently clocked sections on a single device; also described are the effects of spurious difference-frequency components in the C3D output spectrum and the asynchronous transfer of signal charge across a frequency boundary.

A. Effects of Incomplete Charge Transfer

To assess the effects of incomplete charge transfer on the performance of the 20-input four-section C3D electronic lens presented in Chapter IV, this device is modeled as a 4×20 array of individual CCD delay lines, each characterized by the number of bits in the delay-line section, the clock frequency applied to the section, and knowledge of incomplete charge transfer per transfer as a function of clock frequency. Because the cascade charge-coupled device (C3D) lens is fabricated on a single integrated-circuit die, good matching of incomplete charge transfer vs clock frequency across the entire array is expected. Consequently, it is assumed that a single transfer inefficiency vs clock-frequency relationship applies to all of the time-delay sections in the C3D electronic lens.

The position of each delay line within the C3D lens is identified by the subscripts i,j, where $i = 1,2,3,4$ refers to the four clocked sections and $j = -9,-8,\ldots,-0,+0,+1,\ldots,+8,+9$ refers to the transducer

channel position numbered from left to right across the lens.† Based on this notation, the time delay applied to the j^{th} transducer channel (assuming ideal delay lines) is

$$\Delta T_j = \sum_{i=1}^{4} \Delta T_{i,j} = \sum_{i=1}^{4} \frac{N_{i,j}}{F_i} \tag{5.1}$$

where F_i is the clock frequency applied to the i^{th} delay section and $N_{i,j}$ is the number of bits in the i^{th} clock section of the j^{th} transducer.

Recalling the dispersion relations of Joyce and Bertram [5.1] as expressed in Eqs. (4.4) and (4.5), attenuation A_j and time delay ΔT_j for each transducer channel can be defined as

$$A_j = \prod_{i=1}^{4} A_{i,j} = \prod_{i=1}^{4} \left(1 - \epsilon_{F_i}\right)^{2N_{i,j}} \left\{ \exp\left[2N_{i,j} \epsilon_{F_i} \cos\left(\frac{2\pi \nu_{sig}}{F_i} \right) \right] \right\} \tag{5.2}$$

and

$$\Delta T_j = \sum_{i=1}^{4} \Delta T_{i,j} = \sum_{i=1}^{4} \left\{ \frac{N_{i,j}}{F_i} + \frac{N_{i,j} \epsilon_{F_i}}{F_i} \left[\operatorname{sinc}\left(\frac{2\nu_{sig}}{F_i} \right) \right] \right\} \tag{5.3}$$

where ϵ_{F_i} is charge-transfer inefficiency at the clock frequency applied to the i^{th} section of delay. Although these expressions for attenuation and time delay are significant, the variation of these quantities from transducer to transducer rather than their absolute magnitude will determine overall image quality. As a result, the following subsections will examine the effects of attenuation and time-delay variations across the array caused by incomplete charge transfer. Because beam

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†The subscripts $j = -0$ and $j = 0$ refer to the two center transducers of an array containing an even number of transducers. In this context, the "transducer at $j+1$" is located next to the transducer at position j (if $j = -0$, then $j+1 = 0$).

steering and focusing are generally independent of one another, the impact of such a transfer on each of these functions is considered separately.

1. Beam Steering

For the beam-steering section, Eqs. (5.2) and (5.3) can be rewritten as

$$A_j = \left(1 - \epsilon_{F_3}\right)^{2N_{3,j}} \left(1 - \epsilon_{F_4}\right)^{2N_{4,j}} \exp\left[2N_{3,j}\epsilon_{F_3} \cos\left(\frac{2\pi\nu_{sig}}{F_3}\right)\right]$$

$$\cdot \exp\left[2N_{4,j}\epsilon_{F_4} \cos\left(\frac{2\pi\nu_{sig}}{F_4}\right)\right] \tag{5.4}$$

and

$$\Delta T_j = \frac{N_{3,j}}{F_3} + \frac{N_{4,j}}{F_4} + \frac{N_{3,j}\epsilon_{F_3}}{F_3}\left[\text{sinc}\left(\frac{2\nu_{sig}}{F_3}\right)\right]$$

$$+ \frac{N_{4,j}\epsilon_{F_4}}{F_4}\left[\text{sinc}\left(\frac{2\nu_{sig}}{F_4}\right)\right] \tag{5.5}$$

Maintaining the beam-steering convention (established in Chapter IV) that the number of bits in each of the beam-steering sections increases or decreases by an increment of n_3 bits per transducer channel, the recursive relations that express the attenuation and time delay of transducer channel $j+1$ in terms of channel j are

$$A_{j+1} = A_j\left\{\left(1 - \epsilon_{F_3}\right)^{2n_3} \left(1 - \epsilon_{F_4}\right)^{-2n_3}\right.$$

$$\left.\cdot \exp\left[2n_3\epsilon_{F_3} \cos\left(\frac{2\pi\nu_{sig}}{F_3}\right) - 2n_3\epsilon_{F_4} \cos\left(\frac{2\pi\nu_{sig}}{F_4}\right)\right]\right\} \tag{5.6}$$

and

$$\Delta T_{j+1} = \Delta T_j + \frac{n_3}{F_3} - \frac{n_3}{F_4} + \frac{n_3 \epsilon_{F_3}}{F_3}\left[\text{sinc}\left(\frac{2\nu_{sig}}{F_3}\right)\right]$$

$$- \frac{n_3 \epsilon_{F_4}}{F_4}\left[\text{sinc}\left(\frac{2\nu_{sig}}{F_4}\right)\right] \qquad (5.7)$$

Equation (5.6) indicates that the attenuation at any two adjacent transducers will differ by a constant multiplicative factor that will be dependent on the clock frequencies and on the transfer inefficiencies at those frequencies but will be independent of the absolute position along the transducer array. This type of signal attenuation is analogous to the tissue attenuation discussed in Chapter III.B.1. Evaluation of Eq. (3.43) for a 20-element array of 1.5-mm 1.5-MHz transducers steered to an angle of 25° off-axis resulted in an element-to-element attenuation factor based on a tissue absorption of 0.898. If the C3D lens is used to steer the same array to 25° with F_3 = 5 MHz ($\epsilon_5 \approx 0.002$) and F_4 = 30 MHz ($\epsilon_{30} \approx 0.025$), the element-to-element attenuation coefficient is 0.995. This demonstrates that, even for broad differences in charge-transfer inefficiency caused by the large clock-frequency variation required to beam steer to the extremes of the field of view, the change in attenuation across the array resulting from incomplete charge transfer is substantially less than that resulting from acoustic path-length differences.

Comparison of Eq. (5.7) to the beam-steering angle/clock-frequency relation for ideal delay lines [Eq. (4.13)] reveals that the beam-steering angle in the presence of incomplete charge transfer θ_ϵ is

$$\theta_\epsilon = \sin^{-1}\left[\frac{cn_3}{d}\left(\frac{1}{F_3} - \frac{1}{F_4}\right) + \frac{cn_3}{d}\left(\frac{\epsilon_{F_3}\ \text{sinc}\ (2\nu_{sig}/F_3)}{F_3} - \frac{\epsilon_{F_4}\ \text{sinc}\ (2\nu_{sig}/F_4)}{F_4}\right)\right]$$

$$= \sin^{-1}\ (\sin\theta + \sin\Delta\theta) \qquad (5.8)$$

where $\sin\theta$ is the beam-steering angle expected for ideal delay lines and $\sin\Delta\theta$ denotes the small error caused by incomplete transfer. Continuing with the same clock frequencies and transfer inefficiencies as before results in $\theta = 24.62°$ ($\sin\theta = 0.417$), $\sin\Delta\theta = -0.0022$, and $\theta_\epsilon = 24.48°$.

Equation (5.8) therefore indicates that, although incomplete charge transfer will alter the actual beam-steering angle slightly, the lateral resolution and sidelobe level of the image point will not be affected by such time-delay variations. Because transfer inefficiency is well matched at any given clock frequency on the single-chip lens, the device can be operated at clock frequencies much higher than would be normally expected, based on the completeness of charge transfer at these higher frequencies. As indicated in the left portion of Fig. 5.1, the time delay error due to incomplete charge transfer is directly proportional to the number of bits clocked at each frequency, so good matching of transfer efficiency results in a net time delay error that varies linearly across the array for the beam steering section shown.

Implementation of electronic beam steering with a number of individual CCDs, as shown in the right portion of Fig. 5.1, will not provide an assurance of well matched transfer efficiency between devices. As a result, the time delay errors developed across the array due to incomplete charge transfer will be randomly distributed and will tend to degrade the sidelobe suppression afforded by the imaging system. Increased angular beam-steering accuracy and increased sidelobe suppression calls for CCDs with low transfer inefficiency at high clock frequencies if electronic beam steering is realized using individual CCD delay lines.

In addition to substantially reducing the delay line hardware required for electronically beam steered ultrasonic imaging, the C3D single-chip lens provides increased angular beam-steering accuracy because of improved matching of time delay between transducer channels. Furthermore, improved matching of time delay should make it possible to achieve greater degrees of sidelobe suppression with the C3D single-chip lens as compared to individual CCD delay lines.

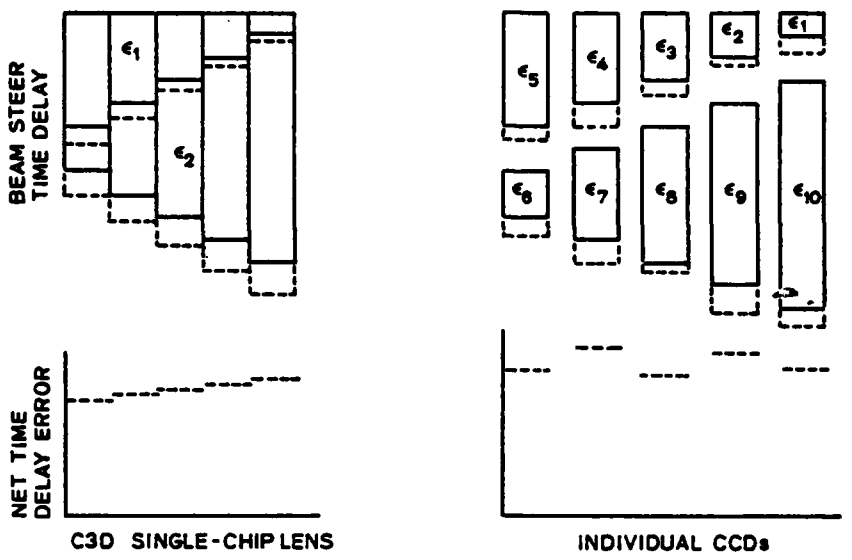

Fig. 5.1. C3D SINGLE-CHIP LENS VS INDIVIDUAL CCDs. (Ideal Time Delay ——; Including Transfer Inefficiency ---)

2. Focusing

Based on the above method, attenuation and time delay produced by the focusing rather than the beam-steering section can be written as

$$A_j = \left(1 - \epsilon_{F_2}\right)^{n_2 j'} \left(1 - \epsilon_{F_1}\right)^{n_1 (j'_{max} - j')} \exp\left[n_2 j' \epsilon_{F_2} \cos\left(\frac{2\pi \nu_{sig}}{F_2}\right)\right]$$

$$\cdot \exp\left[n_1 (j'_{max} - j') \epsilon_{F_1} \cos\left(\frac{2\pi \nu_{sig}}{F_1}\right)\right] \qquad (5.9)$$

and

$$\Delta T_j = \frac{n_2 j'}{2F_2} + \frac{n_1 (j'_{max} - j')}{2F_1} + \frac{n_2 j'}{2F_2} \epsilon_{F_2} \operatorname{sinc}\left(\frac{2\nu_{sig}}{F_2}\right)$$

$$+ \frac{n_1 (j'_{max} - j')}{2F_1} \epsilon_{F_1} \operatorname{sinc}\left(\frac{2\nu_{sig}}{F_1}\right) \qquad (5.10)$$

where

$$j' = |j|^2 + |j|$$

$$j'_{max} = |j_{max}|^2 + |j_{max}|$$

In contrast to the beam-steering section where large differences in frequency are required to steer the array to the extremes of the field of view, focusing over the entire range requires clock frequencies F_1 and F_2 to differ only slightly. Because $\epsilon_{F_1} \approx \epsilon_{F_2}$ for $F_1 \approx F_2$, it is assumed that A_j will also vary by only a small amount across the transducer array and that ΔT_j will nearly equal those values expected for ideal delay-line performance. To verify this assumption, ΔT_j was calculated for the 20-element array of 1.5-mm 1.5-MHz transducers using $F_1 = 8$ MHz ($\epsilon_{F_1} = 0.004$) and $F_2 = 10$ MHz ($\epsilon_{F_2} = 0.006$). Under these conditions, ideal delay lines would focus to a range of 12.0 cm; including the effects of incomplete charge transfer results in a focal point located at 12.05 cm.

The effects of incomplete charge transfer on the operation of the C3D demonstrate that the variation in attenuation across the array is deterministic and insignificant when compared to variations in attenuation caused by tissue absorption within the body. Differences in time delay across the array resulting from incomplete charge transfer shift the focal point of the imaging system in both range and beam-steering angle but do not degrade the lateral resolution or sidelobe response of the focal point. Even at moderately high values of charge-transfer inefficiency, however, spatial shifting of the focal point is slight when compared to lateral resolution or depth of focus. This insensitivity to incomplete charge transfer is a direct result of good transfer-efficiency matching (at any clock frequency) across the array which, in turn, is due to the C3D single-chip lens approach.

B. Effects of Asynchronous Charge Transfer

In the above analysis, it was assumed that the C3D lens could be modeled as a number of independent delay lines and, therefore, any possible charge interactions at the boundary between two sections driven at

different frequencies were neglected. The remainder of this chapter will examine the transfer of charge across a frequency boundary. The generation of frequency components outside the desired signal passband and their impact on imaging-system performance will be investigated, and consideration of the effects of asynchronous charge transfer on the signal will include frequency shifts and time-delay error.

1. Generation of Difference-Frequency Components

Chapter IV suggested that charge from a CCD section being clocked at frequency F_A transferred directly into an adjacent section being clocked at F_B results in the generation of spurious signal components found at the difference frequency $|F_B - F_A|$ and at a number of harmonics of this frequency. To simplify the analysis of asynchronous charge transfer, consider Fig. 5.2 where charge from an electrode pair (1/2-bit CCD delay line) clocked at F_A is transferred into an electrode pair driven at F_B. To further simplify, a uniform background charge (rather than a signal frequency) of Q_o carriers will be transferred into storage well 1 each time F_A undergoes a high-low (falling edge) transition.

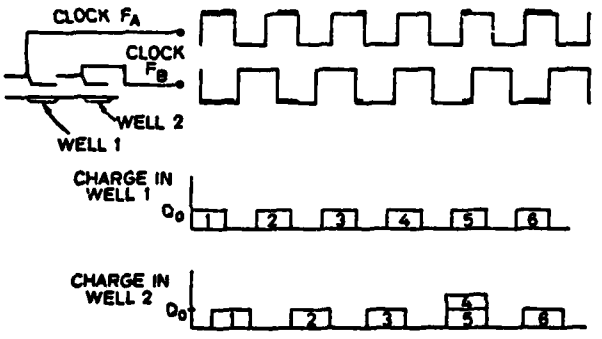

Fig. 5.2. ASYNCHRONOUS TRANSFER OF "FAT ZERO" BACKGROUND CHARGE.

As delineated by the accentuated clocking waveforms in Fig. 5.2, charge can be transferred from storage well 1 into storage well 2 only when F_A is high and F_B is low. As a result, charge transfer can

be initiated either at the rising edge of F_A (when F_B is low) or at the falling edge of F_B (when F_A is high). Under these conditions, the time allowed for charge transfer can vary greatly, depending on the timing of F_B relative to that of F_A; however, even if the time allowed for charge transfer is very short, the majority of charge will be transferred successfully because of the large self-induced fields present during the early stages of the transfer [5.2,5.3]. It will be assumed, therefore, that all of the charge in storage well 1 will be transferred into well 2 even if the time "window" is short. Because an asynchronous transfer can occur only three times in any transducer channel of the four-section C3D lens, the meaning of "all of the charge" in the above assumption can be made less rigid because a slight amount of incomplete charge transfer will not be multiplied repeatedly as it is in the numerous "normal" transfers encountered from input to output.

A critical feature in Fig. 5.2 is that, when $F_B < F_A$, there will be intervals when a packet of charge in well 1 will not have been transferred into well 2 by the time a second packet of charge is transferred into well 1; therefore, the asynchronous transfer of charge across a frequency boundary results in the nonuniform distribution of the originally uniform background charge. The repetition period (the inverse of the fundamental frequency) of this spurious signal component is the lowest common multiple of the periods of F_A and F_B. As a consequence, if F_A and F_B are both multiples of F_{inc}, the maximum repetition period will be $1/F_{inc}$ which, in turn, implies that the spurious signal components will occur at F_{inc} and its harmonics. If F_1 and F_2 are also multiples of $2F_{inc}$, the fundamental frequency of the spurious signal components will be $2F_{inc}$ rather than F_{inc}.

When $F_B > F_A$, a similar nonuniform distribution of the uniform bias charge Q_o occurs, which again results in the generation of spurious signal components whose fundamental frequency will be F_{inc} if F_A and F_B are multiples of F_{inc}. The unwanted signal, however, would be the result of transferring an empty well out of storage well 2 before it has been filled by a transfer from well 1.

Figure 5.3 is the resulting output spectrum of a uniform bias charge that has been transferred across a clock-frequency boundary when

both F_A and F_B are multiples of F_{inc}. Generally, F_{inc} should be chosen so that the resultant "comb" spectrum does not interfere with the desired signal passband. As a result, F_{inc} should be larger than the system bandwidth required to achieve a given axial resolution but sufficiently small to generate enough clock frequencies (for a given F_{max}) to scan the entire field of view. The ultrasonic center frequencies that fall in the middle of the regions free from spurious signals, thereby allowing for the maximum bandwidth on either side of the center frequency, are

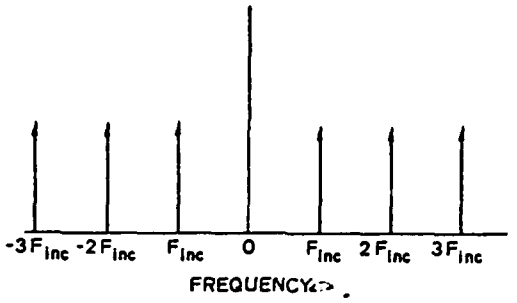

Fig. 5.3. OUTPUT-FREQUENCY SPECTRUM OF BIAS CHARGE AFTER ASYNCHRONOUS TRANSFER.

$$\nu_o = \left(m - \frac{1}{2}\right) F_{inc} \tag{5.11}$$

where $m = 1,2,3,\ldots$. *Because the maximum bandwidth under these conditions is* $B_{max} = F_{inc}$, Eq. (5.11) provides the means to select F_{inc} and m (the number of spurious signal components that occur at frequencies lower than the carrier frequency). Alternatively, the ratio of maximum signal bandwidth to ultrasonic carrier frequency is

$$\frac{B_{max}}{\nu_o} = \frac{F_{inc}}{(m - 1/2)\ F_{inc}} = \frac{1}{(m - 1/2)} \tag{5.12}$$

To achieve a large fractional bandwidth, therefore, m should be minimized which, referring to Eq. (5.11), implies that F_{inc} should be as large as possible for a given center frequency. As observed in Chapter IV, F_{inc} must be small enough to enable the selection of an appropriate number of scan angles to image the entire field of view. For $\nu_o = 1.5$ MHz, $F_{inc} = 1$ MHz $(m = 2)$ is appropriate.

2. Effects on Signal-Frequency Components--Single Channel

The above section examined the generation of spurious signal components resulting from the asynchronous transfer of charge across a frequency boundary. For ultrasonic imaging applications, however, the effect of asynchronous charge transfer on echo returns should be investigated; amplitude accuracy, time-delay accuracy, and freedom from frequency shifts must be characterized to determine the ability of the C3D lens to produce high-quality ultrasonic images.

Figure 5.4 plots a sinusoidal signal frequency ν_{sig} transferred from a storage well clocked at F_A into a storage well clocked at F_B. As indicated by the numbered arrows, the transfer of signal-charge packets across the frequency boundary occurs in three distinct stages.

Stage 1: at the falling edge of F_A, a packet of signal charge is transferred into storage well 1. If a signal charge is already present in well 1, the new packet is added to it. Because there are no storage sites preceding storage well 1 as there are in a real CCD, the size of the charge transferred into well 1 will be the size of the signal waveform at the time when F_A undergoes a high-low transition.

Stage 2: the accumulated charge in storage well 1 will be transferred into storage well 2 at the rising edge of F_A (if F_B is already low) or at the falling edge of F_B (if F_A is already high). This is the actual asynchronous transfer of charge. The time allowed for this transfer is variable; however, because most of the charge is transferred rapidly as the result of self-induced fields, it will be assumed that asynchronous transfer occurs instantaneously. Any charge transferred during this stage will be added to the charge already present in storage well 2.

Stage 3: the accumulated charge in storage well 2 will be transferred out at the rising edges of F_B. In a real CCD, this charge packet will continue to be transferred through a number of storage sites; in this analysis, it will be assumed that the packets leaving storage well 2 constitute the final output signal.

In Fig. 5.4, the signal packets being transferred out of well 2 will depend not only on ν_{sig}, F_A, and F_B but also on the timing of each, relative to the other two. The timing of each waveform can be defined, relative to a common (but arbitrary) time reference (t_{ref} in Fig. 5.4). These three waveforms can be completely specified, therefore, by a frequency and a time delay (expressed as cycles of delay at the given frequency) as

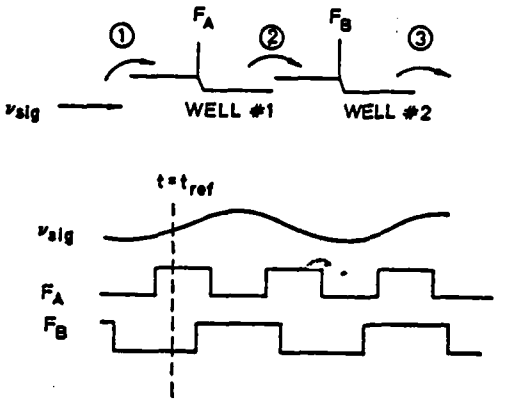

Fig. 5.4. TIMING DIAGRAM OF THE ASYNCHRONOUS TRANSFER OF SIGNAL WAVEFORMS.

$$\text{signal:} \quad A = A_o \sin 2\pi\left[\nu_{sig}(t - t_{ref}) + \Delta_{sig}\right]$$

$$\text{clock 1:} \quad C_1 = C_o \, \text{sgn}\left\{\sin 2\pi\left[F_A(t - t_{ref}) + \Delta_A\right]\right\} \qquad (5.13)$$

$$\text{clock 2:} \quad C_2 = C_o \, \text{sgn}\left\{\sin 2\pi\left[F_B(t - t_{ref}) + \Delta_B\right]\right\}$$

where

$$\text{sgn}(x) = \begin{cases} 1 & \text{if } x > 0 \\ 0 & \text{if } x < 0 \end{cases}$$

Because of the asynchronous character of the transfer of charge from storage well 1 to well 2, it is difficult to derive an analytical expression for the output pulse train emerging from well 2. For any set of frequencies (ν_{sig}, F_A, and F_B) and relative timing information (Δ_{sig}, Δ_A, and Δ_B), however, the sequence of output pulses expected from storage well 2 can be generated (based on the rules and assumptions presented earlier in this section) for the three-stage transfer process. Discrete Fourier transforms (DFTs) may then produce frequency, amplitude,

and phase information concerning the pulse-output sequence. Because the DFT assumes that the sample record is repeated ad infinitum, the record length should contain an integer number of cycles of the input signal and the two clocks. For a signal frequency of 1.5 MHz (period = 0.667 μsec) and clock frequencies of integer multiples of 1 MHz (maximum period = 1.0 μsec), for example, record lengths that are multiples of 2 μsec are appropriate.

Figure 5.5 illustrates the output amplitude and phase of the signal components of a pulse train that has undergone asynchronous transfer as calculated by a 4096-point DFT [5.4] of a 16 μsec record; the test conditions were $\nu_{sig} = 1.5$ MHz, $\Delta_{sig} = 0$, $F_A = 8$ MHz, $\Delta_A = 0$, $F_B = 10$ MHz, and $\Delta_B = 0$. Apparent in the figure are the clock difference-frequency components described in Section B.1 that appear at 2,4,... MHz, the signal-frequency component at 1.5 MHz, and the mixing products between the signal and various difference frequencies that occur at 0.5, 2.5,3.5,... MHz. The calculated frequency spectrum actually continues beyond the 10 MHz limit in Fig. 5.5. The 0 dB level was chosen as the largest in the output spectrum--the F_B clock-frequency component at 10 MHz.

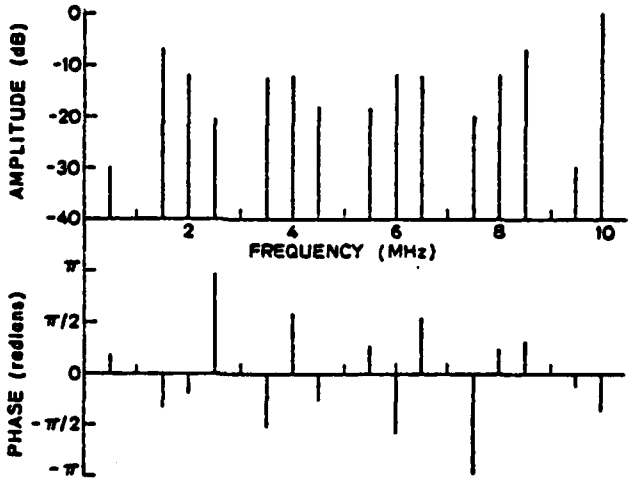

Fig. 5.5. OUTPUT-FREQUENCY SPECTRUM OF 1.5 MHz SIGNAL AFTER ASYNCHRONOUS TRANSFER.

Figure 5.6 presents the simulated amplitude and phase of the 1.5 MHz signal when the timing of clock 2 was shifted relative to that of clock 1 by varying Δ_B and leaving all other parameters constant. The shaded portion indicates that the phase of the emerging 1.5 MHz signal was in the range of $0.3375\pi \pm 0.0375\pi$ rad which, for a 1.5 MHz signal initially at zero phase, corresponds to a time delay through asynchronous transfer of 0.1125 ± 0.0125 μsec. Simulations over a wide range of Δ_B revealed that the probability distribution of time delay within this region is uniform and that no time delays occur on either side of the specified time-delay band. The output amplitude was constant for all values of Δ_B.

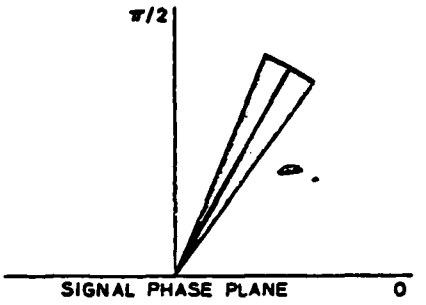

Fig. 5.6. PHASE PLANE REPRESENTATION OF TIME DELAY AND AMPLITUDE UNCERTAINTY CAUSED BY ASYNCHRONOUS TRANSFER.

In the above example, the mean time delay of 0.1125 μsec is the sum of one-half the clock period of F_A and one-half the clock period of F_B. This is the "ideal" time delay that could be expected, based on the observation that Fig. 5.4 represents one-half bit of delay at F_A followed by one-half bit of delay at F_B. In addition, the minimum time delay through the structure is equal to the period of the higher clock frequency (F_B = 10 MHz), and the maximum time delay is equal to that of the lower clock frequency. It can be seen intuitively by examining the waveforms in Fig. 5.7 that the maximum time-delay uncertainty is equal to the difference between the periods of F_A and F_B. The heavy lines denote the times allowed for charge transfer from storage well 1 to well 2, and the dashed lines indicate that waveform 2 can be translated in time with respect to clock 1 without

Fig. 5.7. TIME-DELAY UNCERTAINTY PRODUCED BY RELATIVE TIME SHIFTS OF CLOCKING WAVEFORMS.

affecting the positions of the charge transfers. The maximum amount of shift (and thus timing uncertainty), therefore, is the difference between the two clock periods.

In the above example, clock frequencies were even multiples of 1 MHz and resulted in difference frequencies spaced at 2 MHz intervals. If one clock frequency is an odd multiple of 1 MHz and the other is even, however, the difference frequencies will occur at 1 MHz intervals; this is important because the 1.5 MHz signal frequency can then mix with the difference-frequency component at 3 MHz. One of the mixing products will occur at 1.5 MHz where it will be added as a vector to the desired 1.5 MHz signal, thereby resulting in greater time-delay and amplitude errors. This mixing is illustrated in the DFT output spectrum in Fig. 5.8 at clock frequencies of 8 and 9 MHz. In this simulation, signal frequency has been offset to 1.56 MHz to emphasize that it is indeed a mixing operation with the 3 MHz difference-frequency component that produces the additional signal component at 1.44 MHz. Further simulation reveals that the phase angle of the mixing product will vary throughout 2π rad even though that of the actual signal component may only vary by

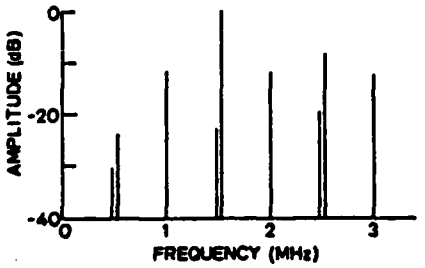

Fig. 5.8. OUTPUT SPECTRUM OF 1.56 MHz SIGNAL, INCLUDING MIXING WITH A 3 MHz COMPONENT.

$$2\pi\nu_{sig}\left|\frac{1}{F_B} - \frac{1}{F_A}\right|$$

The time delay and amplitude uncertainty of the resulting composite signal (Fig. 5.9) will be far worse than the time-delay uncertainty caused by asynchronous transfer in the absence of such mixing. The addition of the mixing product to the desired signal creates uncertainty in the amplitude of the composite signal, whereas asynchronous transfer only introduces phase uncertainty in the desired signal.

It is evident from the above example that the best time delay and amplitude accuracy can be achieved if the clock-frequency increment F_{inc} is such that none of the spurious difference-frequency components is twice the desired signal frequency ν_{sig}. With this restriction, F_{inc} = 1 MHz for a signal frequency of 1.5 MHz (see Section B.1) is no longer appropriate; however, when F_{inc} = 2 MHz, the mixing of signal and difference frequencies can be avoided.

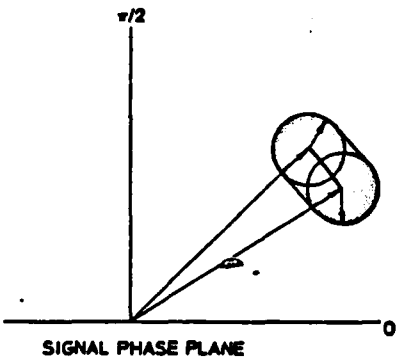

Fig. 5.9. TIME DELAY AND AMPLITUDE UNCERTAINTY WHEN MIXING OCCURS.

Table 5.1 demonstrates the results of introducing different signal frequencies and phase angles into the asynchronous-transfer simulator based on the assumption that F_A and F_B are accurate and stable at all times. The striking feature of this simulation is that the time delay of these signals is a constant, independent of signal frequency and initial signal phase even though it is not equal to the ideal time delay of 0.1125 μsec.

3. Effects on C3D Time Delay and Imaging Performance

In the above section, the discrete Fourier transform was used to determine the effect of signal-charge transfer across a frequency boundary. This section will extend the results obtained to estimate the overall time-delay accuracy in a complete C3D lens containing several frequency boundaries in a number of parallel channels. This estimation will then be applied to assess the maximum level of sidelobe suppression via the CCD approach.

The basic properties of the asynchronous charge transfer for a single channel are summarized as follows.

- There is no shift in signal frequency when crossing a clock-frequency boundary.

- The output amplitude will be a constant, independent of the relative timing (Δ_A, Δ_B) of the two clock frequencies.
- The time delay across the frequency boundary has a maximum uncertainty equal to the difference between the periods of the two clock frequencies. The probability density function within this time-delay window is uniform for randomly selected values of Δ_A and Δ_B. If F_A, F_B, Δ_A, and Δ_B are exact and time independent, however, the time-delay error will also be time independent.

Table 5.1

TIME DELAY ACROSS A FREQUENCY BOUNDARY VS INPUT-SIGNAL FREQUENCY AND PHASE

ν_{sig} (MHz)	Input Phase (rad)	Output Phase (rad)	Net Time Delay (μsec) (input phase-output phase)/ $2\pi \cdot \nu_{sig}$
1.5	0	-0.34π	0.112
1.5	0.25π	-0.09π	0.112
1.5	0.50π	0.16π	0.112
1.5	0.75π	0.41π	0.112
1.5	1.0π	0.66π	0.112
1.5	1.25π	0.91π	0.112
1.5	1.50π	1.16π	0.112
1.5	1.75π	1.41π	0.112
1.75	0	-0.39π	0.112
1.75	0.25π	-0.14π	0.112
1.75	0.50π	0.11π	0.112
1.75	0.75π	0.36π	0.112
1.75	1.0π	0.61π	0.112
1.75	1.25π	0.86π	0.112
1.75	1.50π	1.11π	0.112
1.75	1.75π	1.36π	0.112

Assuming that perfectly stable clocking waveforms can be applied to the various sections of the C3D lens, the time-delay errors associated with each transducer channel will be identical and, as discussed in Chapter III, an error common to each transducer will not degrade the quality of the image point. A reasonable estimate of the degree of clock stability necessary to ensure constant time-delay errors is based on the fact that the relative timing between two clock frequencies (Δ_A and Δ_B) cannot change by an appreciable fraction of the difference between the periods of F_A and F_B during the interval required for a signal to pass through the entire CCD. The ratio of the maximum time-delay error to duration a signal is in the CCD produces a good estimate of clock stability S. If the maximum error is assumed to be 1 percent of the difference between the clock periods, then S is

$$S = \frac{0.01\left|(1/F_A) - (1/F_B)\right|}{(N/2)\left[(1/F_A) + (1/F_B)\right]} = \frac{0.02}{N}\frac{\left|F_A - F_B\right|}{(F_A + F_B)} \tag{5.14}$$

where N is the total number of delay bits. If $N = 100$, $F_A = 10$ MHz, and $F_B = 9$ MHz, for example, a stability of $S \approx 10^{-5}$ is required, which implies that

$$\frac{F_A}{F_B} = \frac{10}{9}\left(1 \pm 10^{-5}\right)$$

$$F_A(t) = F_A(0)\left(1 \pm 10^{-5}\right) \tag{5.15}$$

$$F_B(t) = F_B(0)\left(1 \pm 10^{-5}\right)$$

Such stringent demands on the accuracy and stability of F_A and F_B are not easily met, particularly in a system requiring a number of such clocks. In addition, the rising edges of the clock waveforms in a multichannel system must be applied to all channels simultaneously within the time limit of 1 percent of the difference in clock periods. When

$F_A = 10$ MHz and $F_B = 9$ MHz, the maximum timing error is only 0.1 nsec; in a parallel-channel CCD, the charging of the wide storage electrodes can take much longer if polycrystalline-silicon electrodes are employed in the CCD structure. For these reasons, it appears unlikely that the signal-frequency time-delay error can be held constant for all elements in the transducer array.

When clocks fail to meet the above stability requirements, it may be postulated that the time-delay error in each of the channels will be the result of a random selection from the probability density function that describes the time-delay behavior of that particular frequency boundary. Factors that may cause a clock to be considered unstable are

- insufficient clock-frequency accuracy
- clock-frequency "jitter" caused by interactions between a number of different clock frequencies
- rise-time variations resulting from the distributed RC nature of the signal-channel storage electrodes

Under these conditions, the time-delay error of any signal channel at a frequency boundary can be expressed as a zero-mean uniform PDF random variable whose width, expressed as a number of cycles of signal frequency, is

$$\nu_{sig}\left|\frac{1}{F_A} - \frac{1}{F_B}\right|$$

The standard deviation of the time-delay error (again as a number of cycles of signal frequency) associated with the A-B frequency boundary, therefore, is

$$\sigma_{AB} = \frac{\nu_{sig}}{\sqrt{12}}\left|\frac{1}{F_A} - \frac{1}{F_B}\right| \qquad (5.16)$$

In the C3D lens which has several frequency boundaries, the time-delay errors associated with each boundary can be considered independent random variables, based on the same arguments that led to the

conclusion that the errors associated with each signal channel are independent of one another. Because the variance of the sum of independent variables is equal to the sum of the variances [5.5], the total standard deviation of time delay in the C3D lens is

$$\sigma_T = \left[\sum_{AB} (\sigma_{AB})^2\right]^{1/2} = \frac{\nu_{sig}}{\sqrt{12}} \left[\sum_{AB} \left(\frac{1}{F_A} - \frac{1}{F_B}\right)^2\right]^{1/2}$$

$$= \frac{\nu_{sig}}{\sqrt{12}} \left[\left(\frac{1}{F_1} - \frac{1}{F_2}\right)^2 + \left(\frac{1}{F_2} - \frac{1}{F_3}\right)^2 + \left(\frac{1}{F_3} - \frac{1}{F_4}\right)^2\right]^{1/2} \qquad (5.17)$$

Using this equation to determine the standard deviation of time-delay error for any combination of clock frequencies coupled with the tolerance theory in Chapter III, the maximum level of sidelobe suppression can be predicted for each set of clock frequencies and, hence, for each image point. Figure 3.9 has been reproduced in Fig. 5.10, with the addition of the range of time-delay errors predicted by Eq. (5.17). Generally, image points in the center of the field of view ($|\theta| \leq 12°$) will require medium or high clock frequencies without much frequency variation. Most of the image points in this region should achieve ≥ 40 dB of sidelobe suppression if proper apodization is employed. In contrast, near the extremes of the field of view ($12° \leq |\theta| \leq 25°$) where high and low clock frequencies are required in the beam-steering section, the standard deviation of time-delay error tends to be larger so that maximum sidelobe suppression is 30 to 40 dB down.

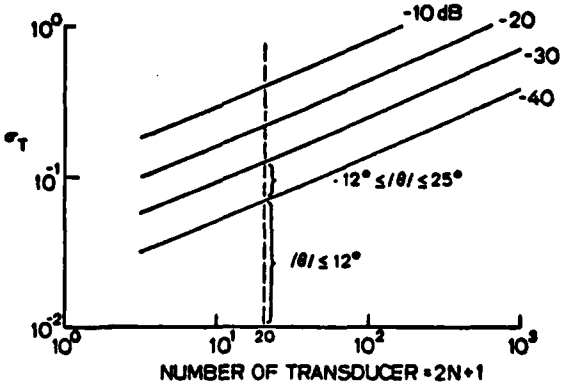

Fig. 5.10. LEVEL OF SIDELOBE SUPPRESSION ACHIEVABLE BECAUSE OF ASYNCHRONOUS CHARGE-TRANSFER TIME-DELAY ERRORS.

The maximum standard deviation can be estimated by assuming that $F_2 = F_{min}$ and that all other clocks are running at high frequency (at the extreme of the field of view). Equation (5.17) can then be approximated by

$$\sigma_{T,max} \approx \frac{\nu_{sig}}{\sqrt{6}\, F_{min}} \tag{5.18}$$

When $\nu_{sig} = 1.5$ MHz and $F_{min} = 6$ MHz, this results in $\sigma_{T,max} \approx 0.1$ which is a worst-case maximum sidelobe-suppression level of better than 30 dB down for a 20-element transducer array.

C. Summary

The fundamental limits of the imaging performance of the C3D electronic lens are set by incomplete charge transfer and the asynchronous transfer of charge across clock-frequency boundaries. Because good matching of transfer efficiency across the monolithic C3D lens is expected, incomplete charge-transfer variations with clock frequency are not expected to affect adversely the resolution or sidelobe level of the resultant image points. Investigation of the asynchronous transfer of charge across a frequency boundary has demonstrated that the generation of spurious signal components will occur at the difference frequencies and at their harmonics of the clock frequencies; however, correct clock-frequency selection can ensure that these spurious signals will not interfere with the desired signal passband. Further analysis revealed that asynchronous transfer introduces slight time-delay errors in the desired signal components. A statistical analysis of these errors coupled with the tolerance theory of random arrays, indicate that their effect will be small enough for the C3D lens to produce images with high degrees of sidelobe suppression.

Chapter V

5.1 W. B. Joyce and W. J. Bertram, "Linearized Dispersion Relation and Green's Function for Discrete-Charge-Transfer Devices with Incomplete Transfer," Bell Syst. Tech. J., 50, Jul-Aug 1971, pp. 1741-1759.

5.2 J. E. Carnes, W. T. Kosonocky, and E. G. Ramberg, "Free Charge Transfer in Charge-Coupled Devices," IEEE Trans. on Electron Devices, ED-19, Jun 1972, pp. 798-808.

5.3 A. M. Mohsen, T. C. McGill, and C. A. Mead, "Charge Transfer in Overlapping Gate Charge-Coupled Devices," IEEE J. Solid State Circuits, SC-8, Jun 1973, pp. 191-207.

5.4 J. A. Greenfield, unpublished work, Stanford University, Stanford, Calif.

5.5 W. B. Davenport, Jr., Probability and Random Processes, McGraw-Hill Book Co., New York, 1970, pp. 244-246.

APPENDIX B: Chapter IV of Michael Eaton's Ph.D. Dissertation

MODELING AND ANALYSIS OF C3D ASYNCHRONOUS CHARGE TRANSFER

The C3D electronic lens is possibly the least understood of the four major components which comprise the preprocessor. Shott [IV-1] has comprehensively examined many aspects pertaining to the design, construction and analysis of the device. However, analysis of asynchronous charge transfer at the internal clock-section boundaries has not been treated. The asynchronous boundary is known [IV-2] to introduce spurious intermodulation products (IPs) at the sum and difference frequencies. This chapter fully analyzes the signal distortions associated with asynchronous charge transfer.

A. C3D Structure

As diagrammed in Figure IV-1, the C3D is a multi-channel charge-coupled device. Each channel is a multiple clock

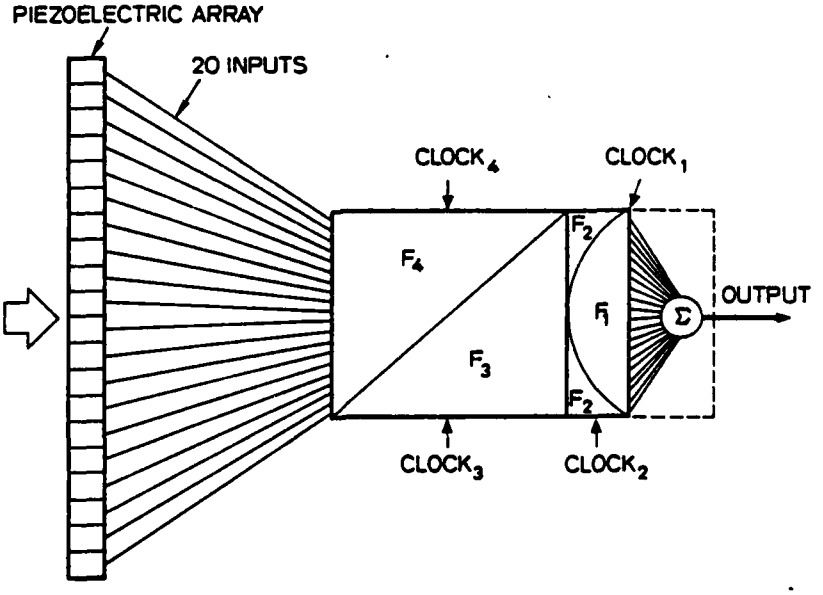

Fig. IV-1. Twenty channel Cascade Charge-Coupled Device (C3D). Each channel has four distinct clock sections.

section CCD--the four portions of the CCD are clocked at different rates. The boundaries (geometry) of the different clock sections are tailored to perform the beam steering and focusing required of an electronic lens. In Figure IV-1, sections 3 and 4 produce a linear time delay (beam steer) while sections 1 and 2 produce a quadratic delay (focus). Summation prior to the output is accomplished by removing the channel-stop diffusions in section 1 and using a common collector diode.

Electronic time delay is performed by dividing an input signal into charge packets which are stored in potential wells under the transfer electrodes [IV-3]. The packets are transferred from one electrode pair to another much like a digital shift register. The transferrals occur in synchrony with the clocking waveform. To relate the charge packets and potential wells to Figure IV-1, the four clock sections, $(F_1,\ldots,F_4)$ may be thought of as similarly shaped sheets of corrugated tin. The troughs run width-wise across the C3D and channel stops run lengthwise to prevent lateral charge flow. C3D clocking makes the corrugations ripple toward the output causing charge transport. In each clock section the rippling transport takes place at a faster or slower rate (depending upon the clock frequency).

Figure IV-2 shows the two-phase overlapping-gate CCD structure that

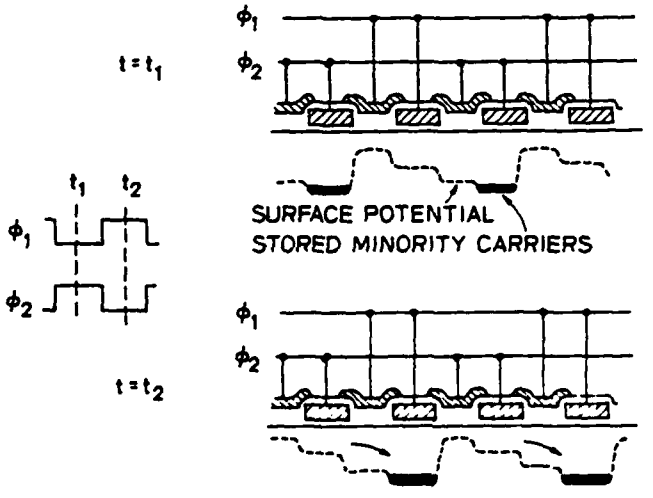

Fig. IV-2. Charge transfer in a two-phase overlapping-gate CCD.

is the basic building block of the C3D electronic lens. Surface-potential wells holding the signal charge are diagrammed for two points on the clocking waveforms. A cross-sectional schematic of one channel of the C3D appears in Figure IV-3, which clearly delineates the internal clock boundaries where asynchronous charge transfer takes place.

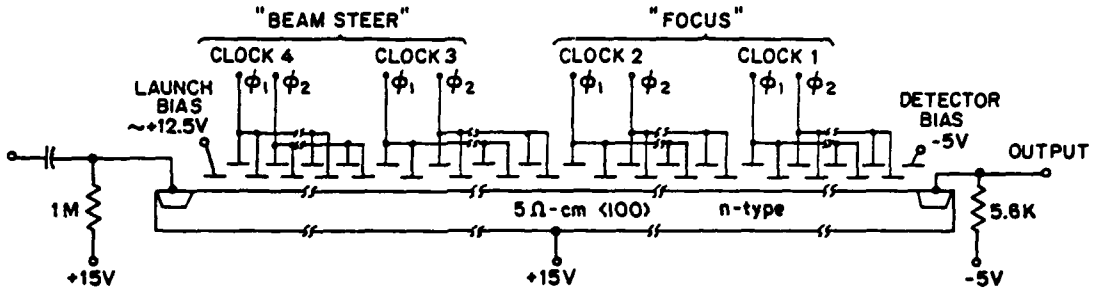

Fig. IV-3. Cross-sectional schematic of the C3D lens showing only one channel. Charge is asynchronously transferred at three internal clock boundaries.

B. Circuit Model of the Asynchronous Interface

A mathematical circuit model of the asynchronous interface is an extremely convenient vehicle for developing intuition as well as providing a foundation for analysis. The asynchronous interface in Figure IV-4a is represented as two abutted CCDs with clock waveforms $c_1(t)$ and $c_2(t)$. Charge is transferred synchronously inside either CCD section and may be represented as a sequence of charge samples with $1/f_i$ spacing, f_i being the respective clock frequency. In this case $q_m(k)$ is the charge sample in the m^{th} storage well at the k^{th} time period. The time function of charge passing through the m^{th} well is the infinite sequence $\{q_m(0), q_m(1), q_m(2), \ldots\}$. Since the samples are uniformly spaced in time, z-transform calculus can be profitably applied. However, at the asynchronous interface the sequence may not be used because of possible asynchronous transfer. Hence, the true time function of charge passing across the interface must be utilized. An expanded view of this interface is shown in Figure IV-4b, where clock waveforms and signal wells are defined.

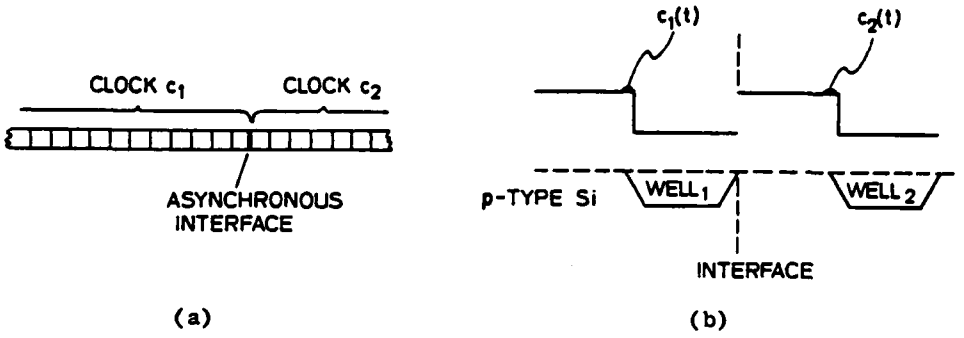

Fig. IV-4. C3D asynchronous interface. (a) Abuttment of two CCDs resulting in asynchronous interface; (b) expanded view of interface defining clock waveforms and potential wells for circuit model.

Each electrode/well ("half-bit") unit in this figure may be analyzed using an equivalent circuit model. Consider the half-bit to the left of the interface in Figure IV-4b. The charge packets flowing into well$_1$ may be represented as an impulsive current generator, $i_1(t)$, pulsing at a rate f_1. Charge flowing out of well$_1$ is represented by a current $i_2(t)$, while the charge stored in that well may be thought of as stored on a capacitor C, (the MOS capacitor above well$_1$). With these definitions the proposed "half-bit" model is shown in Figure IV-5. The model consists of the driving function, $i_1(t)$, which is the synchronous charge transfer into well$_1$; a controlled output current source, $i_2(t)$, and an asynchronous switch, S, which closes whenever $c_2(t) - c_1(t)$ surpasses some threshold T.

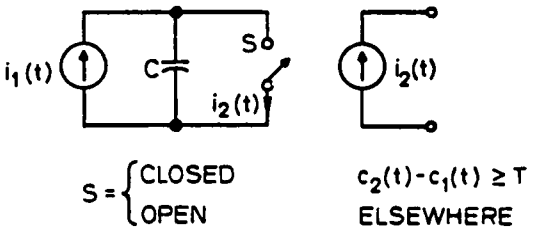

Fig. IV-5. Circuit model of "half-bit" clocked by $c_1(t)$ in Fig. IV-4b. Charge on capacitor C is same as charge stored in well$_1$; $i_s(t)$ represents charge flowing out of well$_1$. Quantities are defined in Fig. IV-4b.

A complete model (Figure IV-6) of the interface is comprised of two cascaded half-bit lumps representing both well$_1$ and well$_2$ of Figure IV-4b. Input

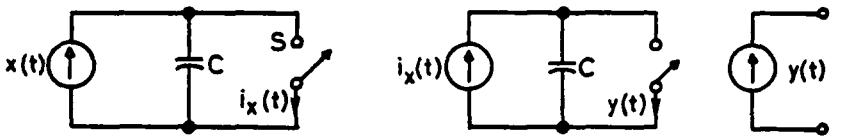

Fig. IV-6. Two-lump circuit model of C3D asynchronous charge transfer. Switch S operates as in Figure IV-5 while second switch closes at a rate f_2. x(t) is the input current; y(t) the output current.

x(t) supplies samples at a constant rate f_1. Switch S operates asynchronously as in Figure IV-5 with an average rate of $f_L = \min(f_1, f_2)$. Current $i_x(t)$ flowing through switch S excites the second lump. The switch in this lump operates synchronously at a rate f_2 resulting in a synchronous output y(t).

Verification of the accuracy of the model is possible with the aid of Figure IV-7, which shows two complete bits on each side of the interface. This interface system has only four stable surface-potential configurations, each a combination of two states: state 0: $c_z\phi_1 > c_z\phi_2$; and state 1: $c_z\phi_2 > c_z\phi_1$. $c_z\phi_w$ are the four clock voltages. States 11 and 10 correspond to current source x(t) supplying an impulse of current to capacitor C while switch S is open. State 01 corresponds to switch S being open and $x = 0$ with some charge on capacitor C. State 00 is the only state possible where S is closed and charge is transferred out of $well_1$. In this idealized model it is important to note that switch S can never be closed while x is supplying current. The reason is that $x \neq 0$ implies $c_1\phi_2 > c_1\phi_1$ (in Figure IV-7) which in turn implies $c_1 \geq c_2$ (in Figure IV-5). Therefore $c_2 - c_1 \leq 0$ and switch S is open by virtue of T being a positive threshold. In summary, the circuit model of Figure IV-6 accurately represents all possible charge configurations at the asynchronous interface.

C. Charge Transfer Analysis: Orthogonal Decomposition

The system/circuit designer interested in applying the C3D is basically concerned with three aspects: (1) frequencies of the spurious components; (2) time delay of the signal; and (3) output amplitude of the signal. Thus, the difficult problem of finding the general time-dependent impulse response of the C3D is circumvented. Since the desired signal component will be filtered at the output, it is sufficient to only determine the frequencies of the interfering components, their amplitudes being unimportant. These interference frequencies can then be avoided and the time delay and amplitude of the output signal component are the only remaining quantities of interest.

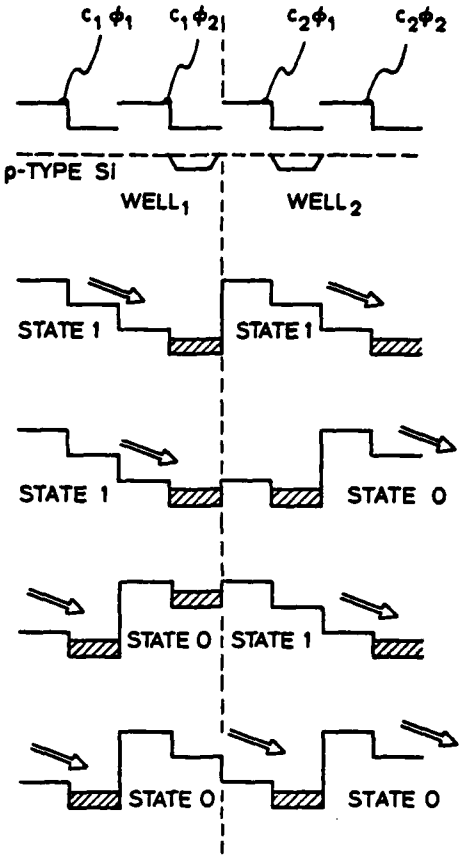

Fig. IV-7. C3D asynchronous interface and the four stable charge configurations. Configurations verify circuit model of Fig. IV-5.

The prime stumbling block in analysis of the model of Figure IV-6 is the asynchronous operation of switch S. If a switching function, s(t), is defined as

$$s = \begin{cases} 1, & S \text{ closed} \\ 0, & S \text{ open} \end{cases}$$

then the switch may be considered as a gate and $s(t) = 1/2\ \{1+ \text{sgn}[c_2(t)-c_1(t)-T]\}$. The easiest way to gain insight into the behavior of $s(t)$ is to consider a simple example such as that in Figure IV-8. $c_2(t)$ is a 5 Hz. square wave, $c_1(t)$ is a 4 Hz. square wave, and T is one half of the square wave amplitude. In this case the gating function

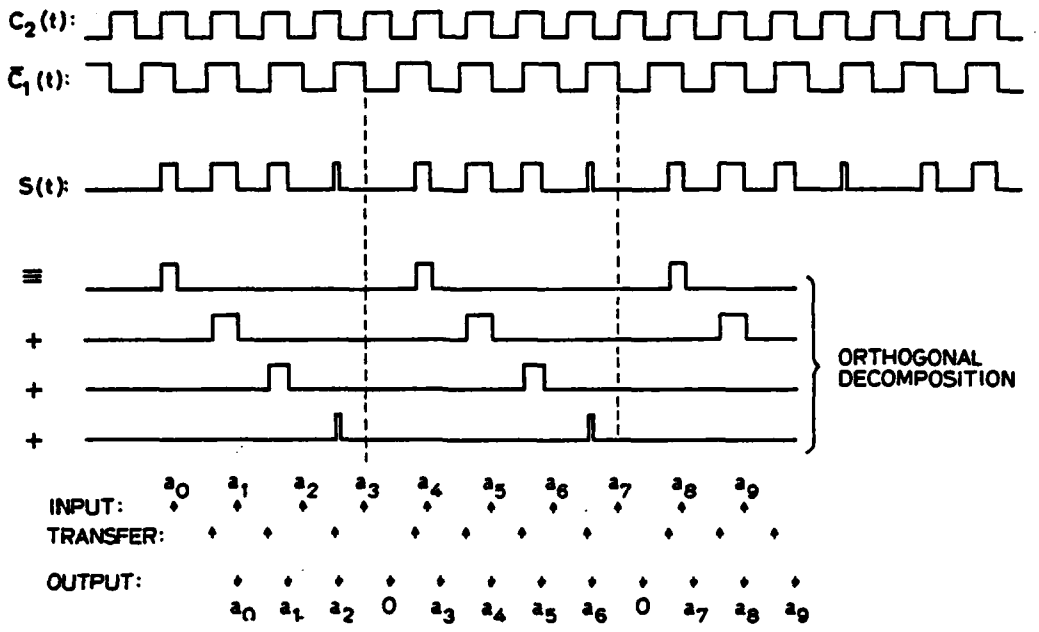

Fig. IV-8. Decomposition of gating function s(t) into orthogonal basis vectors. $c_2(t)$ is a 5 Hz. square wave, $c_1(t)$ a 4 Hz. square wave. s(t) has a 1 Hz. period which is the greatest common denominator (GCD) of 4 and 5.

s(t) is given by $c_2(t).\overline{c_1}(t)$, the dot being interpreted either as multiplication or logical ANDing. The overbar means the logical complement. For ease of graphing, c_2 and $\overline{c_1}$ are plotted, and $s = 1$ iff both $c_2 = 1$ and $\overline{c_1} = 1$. Assuming instantaneous charge transfer [IV-4], the leading edges of s(t) mark the points when the asynchronous transfer occurs. Input pulses occur on the falling edges of $\overline{c_1}(t)$ while output pulses are on falling edges of $c_2(t)$. The figure also shows a sequence of periodic inputs, the transfer sequence across the interface, and the periodic output pulses resulting from the input sequence.

Analysis is facilitated by noting that s(t) may be decomposed into four orthogonal components, each periodic with a common frequency. This is given by the greatest common denominator (GCD) of 4 and 5, which is 1 Hz. Since all components have the same period, the sum is periodic with rate GCD also. Thus, the asynchronous interface is a time-varying system with periodic parameters.

The general analysis of time-varying systems is unwieldy but since the asynchronous interface is a linear system with periodic parameters, we may employ the simplifying theory of Floquet [IV-5]. Briefly, Floquet theory states that if an input of the form $\exp(j2\pi f_o t)$ is applied to a linear, time-varying system with periodic parameters of frequency GCD, the output has the form

$$\sum_{k=-\infty}^{\infty} B_k \exp[j2\pi(f_o+kGCD)t]$$

This situation is shown in Figure IV-9a. In the case of the C3D asynchronous interface, a sinusoidal input is sampled at frequency f_1 (the frequency of clock $c_1(t)$). The corresponding input and output spectra are schematically diagrammed in Figure IV-9b. Assuming both a real input signal, $\cos(2\pi f_o t)$, and dc bias ("fat zero") charge, the output spectrum contains components at frequencies of the form

$$\pm (Zf_o+mf_1+nGCD)$$

where m and n are integers and Z = one or zero.

(a) Continuous Input

(b) Sampled Input

Fig. IV-9. Input and output of linear, time-varying system with periodic parameters for (a) continuous input and (b) sampled input. GCD = parameter rate; f_o = signal frequency; f_1 = sampling frequency.

If $f_1 = pGCD$ where p is an integer, the interference frequency is $\pm[Zf_o+(mp+n)GCD]$. Interference with the desired signal component occurs when

$$f_o = \pm [f_o+(mp+n)GCD]$$

or

$$f_o = \pm (mp+n)GCD$$

which has solutions $kGCD/2$. Therefore the objective of no interference translates into the requirement

$$f_o \neq k \frac{GCD}{2} \qquad k \text{ any integer}$$

For example, if GCD = 1MHz then $f_o \neq 0.5, 1.0, 1.5, 2.0, 2.5, \ldots$ MHz. Thus, GCD = 1MHz is a reasonable choice for $f_o = 2.25$ MHz, a standard ultrasound frequency. It is clear from the above that the maximum bandwidth, BW, of the ultrasound burst is restricted by $BW < GCD/2$ from which the following design inequalities may be obtained:

$$GCD > 2BW$$

$$k \frac{GCD}{2} \notin (f_l, f_u) \cong (f_o - \frac{BW}{2}, f_o + \frac{BW}{2}) \qquad k \text{ any integer}$$

For example, in modern pulse-echo ultrasound

$$BW \sim \frac{f_o}{2}$$

$$\text{then} \quad \begin{cases} GCD > f_o \\ GCD > f_o + \frac{BW}{2} \end{cases}$$

so the value of GCD which simultaneously satisfies both inequalities is $GCD > \frac{5}{4} f_o$. To ensure some guard band, $BW \sim f_o$ would actually be used with

$$GCD > \frac{3}{2} f_o$$

for high resolution systems.

Analytic analysis of the amplitude and time delay of the desired signal component is possible through use of orthogonal decomposition of $s(t)$. Since the interface model of Figure IV-6 consists of two identical circuit lumps, each may first be analyzed independently then later combined. The analysis proceeds by considering the exciting source to be continuous instead of pulsatile. By virtue of linearity, the sampled nature of the input is constructed as a superposition of sinusoidal inputs.

Consider only the first circuit lump of Figure IV-6. Through application of the orthogonal decomposition of $s(t)$, $i_x(t)$ is a train of impulses, which, for our purposes may be represented as

$$i_x(t) = \sum_{i=1}^{L} a_i(t) \sum_{k=-\infty}^{\infty} \delta\left(t - \frac{k}{GCD} - t_i\right)$$

$$= \sum_{i=1}^{L} a_i(t)\ GCD\ comb\ [GCD(t-t_i)]$$

where the L basis vectors have leading edges at the times t_i. Suppose the continous input $x(t) = \exp(j2\pi f_o t)$ is applied. If $\{t_k\}$ is the sequence of switch closures then $a_i(t_k)$ equals the strength of the impulse at $t=t_k$ which also equals the integral of input current between t_k and t_{k-1}. There are only i different intervals between switch closures, call these Δ_i. Then

$$a_i(t_k) = \int_{t_{k-1}}^{t_k} x(t)dt = \int_{t_k-\Delta_i}^{t_k} \exp(j2\pi f_o t)dt$$

$$= \frac{1}{j2\pi f_o}\left\{\exp(j2\pi f_o t_k) - \exp[j2\pi f_o(t_k-\Delta_i)]\right\}$$

$$= \Delta_i \exp(-j\pi f_o \Delta_i)\ sinc(f_o\Delta_i)\ \exp(j2\pi f_o t_k)$$

Thus

$$i_x(t) = \sum_i GCD\Delta_i \exp(-j\pi f_o\Delta_i) sinc(f_o\Delta_i) \exp(j2\pi f_o t)\ comb\ [GCD(t-t_i)]$$

and the Fourier transform of i_x is

$$\mathcal{F}\{i_x\} = \sum_i GCD\Delta_i \exp(-j\pi f_o \Delta_i)\,\mathrm{sinc}(f_o\Delta_i)\,\delta(f-f_o) * \frac{\exp(-j2\pi t_i f)}{GCD}\,\mathrm{comb}\left(\frac{f}{GCD}\right) \tag{IV-1}$$

Equation IV-1 is the general formula for the spectrum of $i_x(t)$ when the input is a continuous sinusoid. However, in the real device $x(t)$ is a sinusoid sampled at rate f_1, i.e.

$$x(t) = \sum_{n=-\infty}^{\infty} \exp[j2\pi(f_o+nf_1)t] \tag{IV-2}$$

Plugging (IV-2) directly into (IV-1) yields

$$\mathcal{F}\{i_x\} = \sum_{i=1}^{L} GCD\Delta_i \left\{ \sum_{n=-\infty}^{\infty} \exp[-j\pi(f_o+nf_1)\Delta_i]\,\mathrm{sinc}[(f_o+nf_1)\Delta_i]\,\delta(f-f_o-nf_1) \right\} * \frac{\exp(-j2\pi t_i f)}{GCD}\,\mathrm{comb}\left(\frac{f}{GCD}\right) \tag{IV-3}$$

Now suppose $f_1 = pGCD$, p an integer, then the transform of IV-3 evaluated at $f = f_o$ is

$$\mathcal{F}\{i_x\}\Big|_{f=f_o} = \sum_{i=1}^{L} GCD\Delta_i \sum_{n=-\infty}^{\infty} \exp\{j\pi[nf_1(2t_i-\Delta_i)-f_o\Delta_i]\}\,\mathrm{sinc}[(f_o+nf_1)\Delta_i] \tag{IV-4}$$

Analysis of the second circuit lump is exactly analogous. The output signal has the form

$$y(t) = \sum_{k=-\infty}^{\infty} b(t)\,\delta\left(t-\frac{k}{f_2}\right) = b(t)\, f_2\, \mathrm{comb}(f_2 t)$$

If $i_x(t)$ is the continuous sinusoid

$$i_x(t) = \exp(j2\pi f_o t)$$

then

$$\mathcal{F}\{y\} = \exp(-j\pi f_o/f_2)\ \text{sinc}\ (\frac{f_o}{f_2})\delta(f-f_0) * \frac{1}{f_2}\ \text{comb}\ (\frac{f}{f_2})$$

The actual input to the second circuit lump is

$$i_x(t) = \sum_{i=1}^{L} \sum_{n=-\infty}^{\infty} \exp(-j2\pi t_i nGCD)\exp[j2\pi(f_o+nGCD)t]$$

and the output spectrum at $f = f_o$ is

$$\mathcal{F}\{y\}\Big|_{f = f_o} = \sum_{i=1}^{L} \sum_{n=-\infty}^{\infty} \frac{f_o}{f_o - nf_2} \exp[j\pi(2t_i nf_2 - f_o/f_2]\text{sinc}(\frac{f_o}{f_2}) \qquad \text{(IV-5)}$$

Therefore the frequency response at the signal frequency f_o is the product

$$H(f_o) = \mathcal{F}\{i_x\}\Big|_{f_o} \cdot \mathcal{F}\{y\}\Big|_{f_o}$$

The conclusion is that the analytical result is mathematically tractable but is too involved for design purposes. A general observation is that the sinc terms indicate that the response falls off as the signal frequency increases--the asynchronous interface behaves as a lowpass filter.

A heuristic approach will be taken to obtain results which are readily useful for design purposes. Time delay through the asynchronous interface is investigated first. Shott [IV-6] has reported the ideal time delay through the interface to be $\frac{1}{2}(\frac{1}{f_1} + \frac{1}{f_2})$. He also found that there is a time delay jitter which depends upon the relative phasing of the two clocks, $c_1(t)$ and $c_2(t)$. The jitter can be seen in the example of Figure IV-10. In this example $f_2 = 4$Hz and $f_1 = 1$ Hz. The ideal delay equals 0.625 sec. In Figure IV-10a the relative clock phasing has been adjusted to produce a time delay, $\tau_d = 0.75$ sec. Two asynchronous transfers per 1/GCD are evident, however only the first is an active transfer. If it is attempted to increase the delay further by slightly advancing the phase of $\overline{c_1}$ as in Figure IV-10b, the delay instead jumps to a minimum value of $\tau_d = 0.5+\epsilon$ sec.

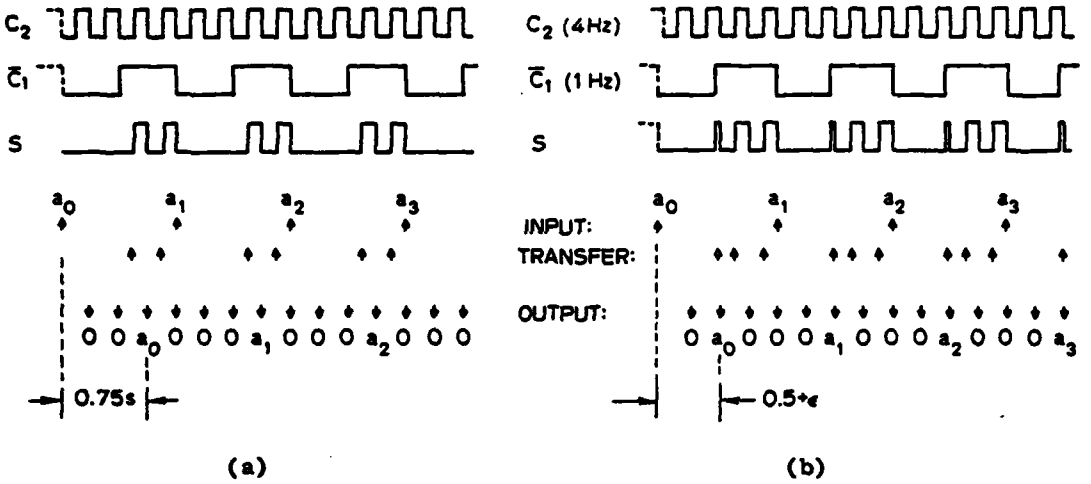

Fig. IV-10. Relative phasing of clocks c_1 and c_2 alters the signal delay through the asynchronous interface. (a) Delay = 0.75 sec; (b) delay = $0.5+\epsilon$ sec.

This happens because a third asynchronous transfer appears at an earlier time than the original transfer, expediting the throughput of the charge sample. The third transfer is a result of the large difference between f_1 and f_2. Careful scrutiny of the effects of changing the relative phase of c_1 and c_2 in Figure IV-10 lead to the conclusion that the peak-to-peak jitter is equal to the difference between the clock periods reduced by a factor proportional to the relative difference between f_1 and f_2. Specifically, if

$$f_L \triangleq \min(f_1, f_2)$$

$$f_H \triangleq \max(f_1, f_2)$$

$$\tau_d(\text{nominal}) \triangleq \frac{1}{2}\left(\frac{1}{f_1} + \frac{1}{f_2}\right)$$

then

$$\tau_d = \frac{1}{2}\left(\frac{1}{f_L} + \frac{1}{f_H}\right) \pm \frac{GCD}{f_H - f_L} \frac{1}{2}\left(\frac{1}{f_L} - \frac{1}{f_H}\right)$$

$$= \frac{1}{2}\left(\frac{1}{f_L} + \frac{1}{f_H}\right) \pm \frac{GCD}{2 f_H f_L}$$

or

$$\tau_d = \tau_d(\text{nominal}) \left[1 \pm \frac{GCD}{f_1 + f_2}\right] \qquad \text{(IV-6)}$$

Thus the jitter is usually substantially smaller than that reported by Shott [IV-6].

Since the above formulation was developed from a heuristic standpoint, a computer simulator was written to test for correctness. The asynchronous transfer algorithm is from Shott [IV-7] and is depicted in Pascal-like notation below.

```
(* t_k are the switch closure times *)
well_1 = well_2 = 0 (* T_1 = input period; T_2 = output period *)
m = n = k = 0
Δ = min (T_1,T_2)/100          (* a "small" initial phase *)

repeat
        time = min(t_k, mT_1 + Δ, nT_2)
        if time = mT_1 + Δ then
                  well_1 ← well_1 + input (m)
                  m ← succ(m)
        if time = t_k then
                  well_2 ← well_2 + well_1
                  well_1 ← 0
                  k ← succ(k)
        if time = nT_2 then
                  output(n) ← well_2
                  well_2 ← 0
                  n = succ(n)
until forever
```

The results of the simulator on a wide variety of clock frequencies, relative phasing and signal frequencies indicates that equation IV-6 accurately predicts the bounds on the peak-to-peak jitter. If the relative clock phase has a uniform distribution then the jitter is also uniform on $(-\frac{GCD}{2f_1f_2}, \frac{GCD}{2f_1f_2})$. Random time delay jitter may be eliminated entirely by phase locking the C3D clocks.

The final topic concerning asynchronous interface is the variation of the output signal amplitude versus both clock and signal frequencies. The equation $s = \bar{\phi}_1 \cdot c_2$ implies that there is at least one asynchronous transfer every $1/f_L$ seconds. Because of this, the half-bit (circuit lump) which clocks at f_L will operate essentially synchronously, that is, charge packets are never added together before being clocked out. The signal therefore undergoes pure time delay in the half-bit section which is clocked at f_L giving rise to two different cases:

Case (i) $f_L = f_1$

Referring to Figure IV-11, the charge samples $i_x(t)$ are essentially delayed versions of $x(t)$, so for amplitude analysis the first lump may be dropped and $i_x(t)$ becomes the input signal. The only portion of the interface model influencing the output signal amplitude is the second lump, shown dotted in Figure IV-11. This circuit is equivalent to a zero-order hold (ZOH) device with a "hold" time of $1/f_2$, and frequency response [IV-8]

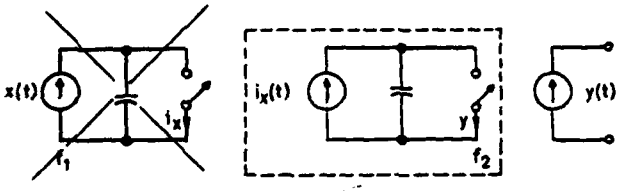

Fig. IV-11. Output amplitude analysis. $f_1 = f_L \triangleq \min(f_1, f_2)$. The second circuit lump is equivalent to a zero-order hold (ZOH) circuit.

$$|H(f_o)| = \text{sinc}\left(\frac{f_o}{f_2}\right) \qquad \text{(IV-7)}$$

The two operations of sampling the model's capacitor voltage and evaluating the sampled spectrum at $f = f_o$ effectively "undo" one another

with the result that equation IV-7 is the overall frequency response of the asynchronous interface when $f_L = f_1$.

Case (ii) $f_L = f_2$

In this case input pulses arriving at the faster rate f_H $(=f_1)$ are averaged in both of the capacitors. However, those not averaged in $well_1$ are averaged in $well_2$ and vice versa with the net effect that the input samples are averaged over a period of $1/f_2$ and then dumped. Once again this constitutes a ZOH device with $1/f_2$ "hold" time and resulting response $|H(f_o)| = \text{sinc}(f_o/f_2)$. The overall amplitude frequency response is the same in both cases and equation IV-7 adequately describes the response of the asynchronous interface for all combinations of clock and signal frequencies as well as relative clock phase.

The computer simulator was again used to check the accuracy of equation IV-7 and the results are plotted in Figure IV-12. Very good agreement was obtained in all cases; the greatest deviation from $\text{sinc}(f_o/f_2)$ behavior was obtained using small values of f_1/GCD and f_2/GCD where there are fewer input samples averaged over the $1/\text{GCD}$ fundamental period.

D. Summary

The important design formulas developed in this chapter are presented together here for easy reference.

Undesirable signal frequencies:

$$f_o \neq k\,\frac{GCD}{2}\,, \qquad k \text{ any integer}$$

Restriction on the greatest common denominator (GCD) of clock frequencies:

$$GCD > 2(BW)$$

$$k\,\frac{GCD}{2} \notin (f_1, f_u) \cong \left(f_o - \frac{BW}{2}\,,\ f_o + \frac{BW}{2}\right)$$

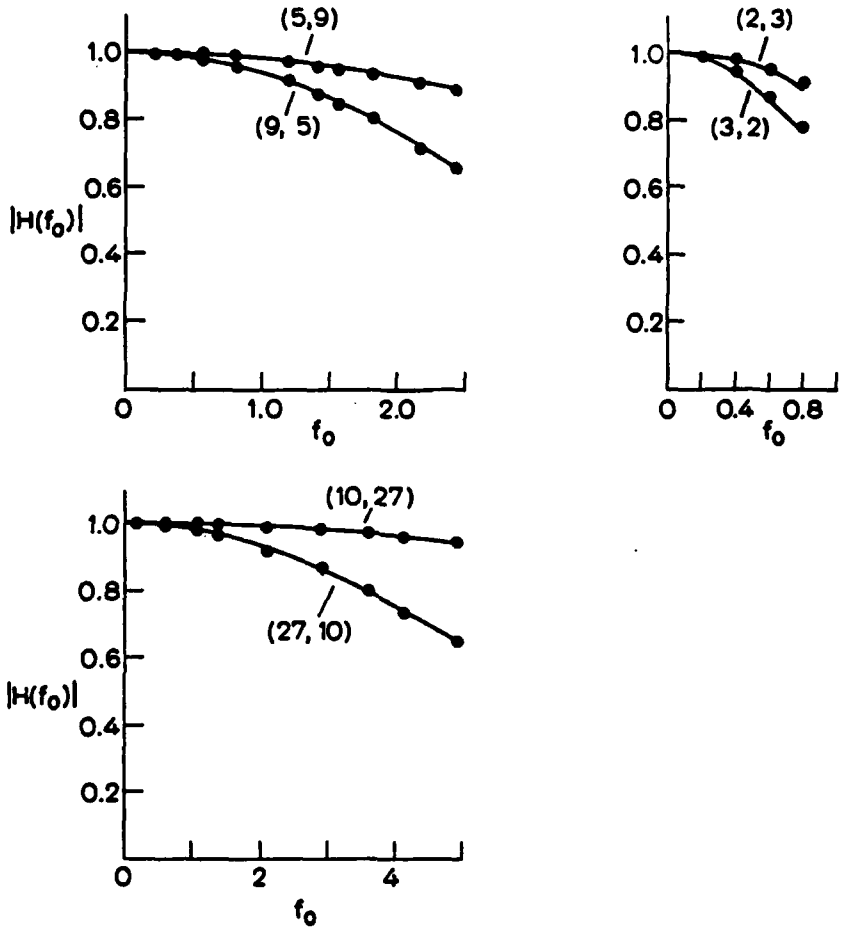

Fig. IV-12. Amplitude frequency response of C3D asynchronous interface for various clock frequency combinations (f_1, f_2). Solid lines are sinc (f_o/f_2); plotted points are output from discrete-transfer computer simulator of interface.

Nominal time delay of asynchronous interface:

$$\tau_d(\text{nominal}) = \frac{1}{2}\left(\frac{1}{f_1} + \frac{1}{f_2}\right)$$

Time delay jitter using unlocked clocks:

$$\tau_d = \tau_d(\text{nominal})\left[1 \pm \frac{GCD}{f_1+f_2}\right]$$

Frequency response of asynchronous interface:

$$|H(f_o)| = \text{sinc}\left(\frac{f_o}{f_2}\right)$$

Several observations may be drawn from these formulas. First, C3D clocking waveforms should be phased-locked to prevent time delay errors which were shown in Chapter III to degrade sidelobe performance. If phase-locking is impractical, then high clock frequencies are preferred which are *noncomposite* numbers, i.e., their GCD is small. However, GCD cannot be decreased too much or the ultrasound bandwidth will be restricted--as usual, an engineering compromise must be struck. Finally, cascaded multiple sections with asynchronous boundaries must respect the penalty paid in SNR as the number of sections increases. In this case, equation IV-7 is useful for C3D design purposes since each boundary behaves as an independent transfer function.

Chapter IV

[IV-1] J.D. Shott, "Charge-Coupled Devices for Use in Electronically Focused Ultrasonic Imaging Systems," Ph.D. dissertation, TR No. 4957-1, Stanford Electronics Laboratories, Stanford University, May 1978.

[IV-2] Ibid, p. 82.

[IV-3] R.D. Melen, J.D. Shott, B.T. Lee and L.C. Granger, "Charge Coupled Devices for Holographic and Beamsteering Sonar Systems," Acoustical Holography, 7, (in press).

[IV-4] J.D. Shott, op cit, p. 83.

[IV-5] H. D'Angelo, Linear Time-Varying Systems: Analysis and Synthesis, Allyn and Bacon, 1970, p. 195.

[IV-6] J.D. Shott, op cit, p. 88.

[IV-7] Ibid, p. 85.

[IV-8] K. Ogata, Modern Control Engineering, Prentice-Hall, 1970, p. 639.